LVDS – LVDS Buffer Evaluation Board

LVDS001EVK Revision 1.0

April 2001

The LVDS – LVDS Buffer Evaluation Board

The LVDS – LVDS Buffer Evaluation Board is used to demonstrate the use and performance of the DS90LV001 device. Input LVDS or LVPECL signals or complementary signals from a signal generator can be probed differentially and output LVDS channels can be probed single-ended or differentially.

The DS90LV001 can be used as a "stub-hider." In many systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the "stub length" or the distance between the transmission line and the unterminated receivers on the individual cards. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns and PCB designs often make it difficult to make the stubs as short as the engineer would like. The DS90LV001, available in the LLP (Leadless Leadframe Package) package, can improve system performance by allowing the receiver to be placed very close to the main transmission line either on the backplane itself or very close to the connector on the card. Longer traces to the LVDS receiver may be placed after the DS90LV001. This very small LLP package is a 75% space savings over the SOIC package.

Shown below in *Figure 1* and *Figure 2* are two typical applications for the DS90LV001, the cable repeater application and the backplane stub-hider application.

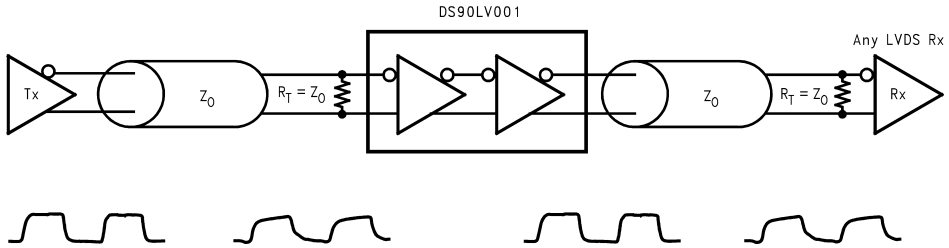


Figure 1: Cable Repeater Application

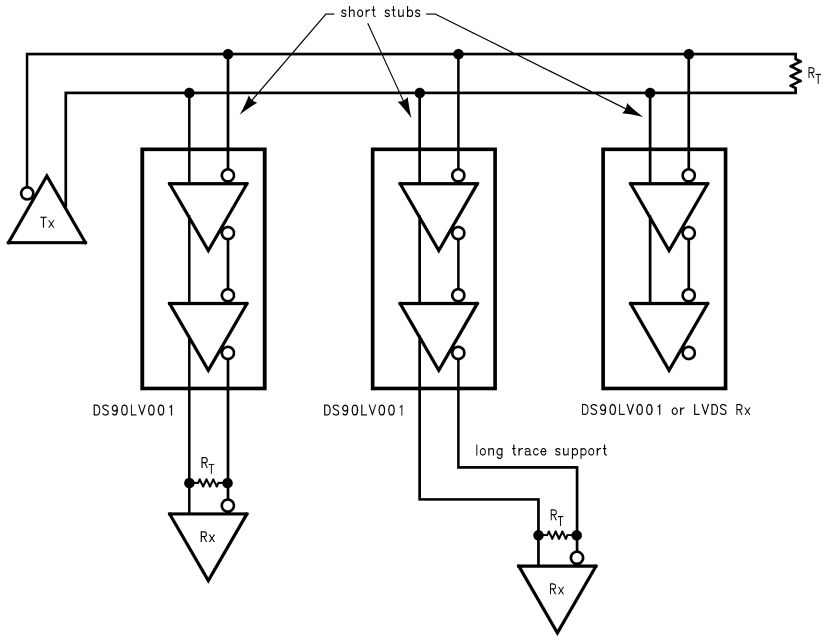


Figure 2: Backplane Stub-Hider Application

Purpose

The purpose of the Low Voltage Differential Signaling (LVDS) Evaluation Printed Circuit Board (PCB) is to allow the user to evaluate the performance of the device. The part number for the Evaluation Kit is LVDS001EVK.

Board Description

The simplified block diagram of this board is shown in *Figure 3* below.

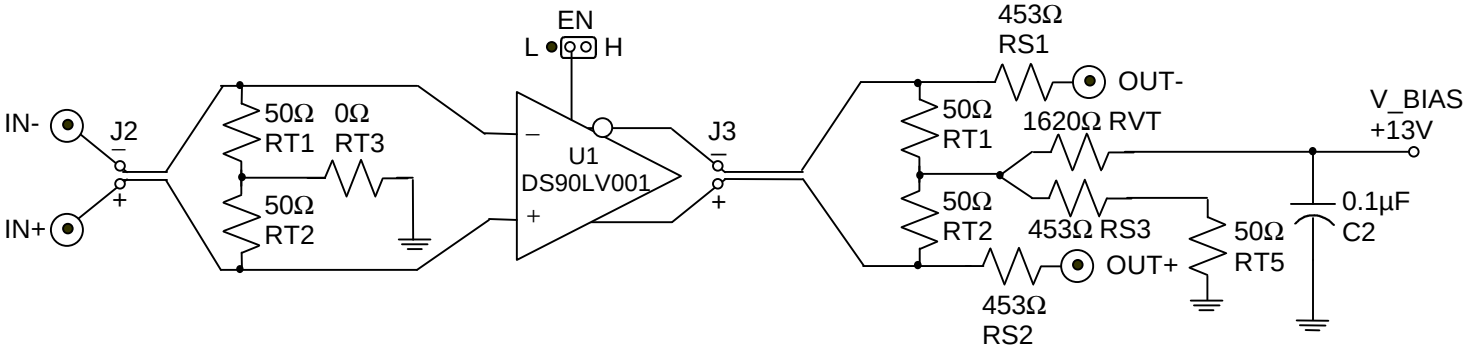


Figure 3: PCB Block Diagram

Termination options on the buffer inputs (IN- and IN+) accommodate either two separate 50 Ohm terminations (RT1 and RT2) (each line to ground when RT3 of 0 Ohms is in place) on the bottom of the board or a 100 Ohm resistor connected across the inputs (differential) when RT3 is removed. The first option allows for a standard signal generator interface. The second option allows for the DS90LV001 to be driven by an LVDS driver. Input signals are connected at test points IN- and IN+. A direct probe connection is possible with a TEK P6247 differential probe high impedance probe (>1GHz bandwidth) on the LVDS signals at test point J2.

The termination load of a standard 100 Ohm differential termination along with series 453 Ohm resistors (RS1 and RS2) are implemented since 50 Ohm probes are employed on the buffer output signal through the SMA connectors OUT- and OUT+. The LVDS driver cannot drive the 50 Ohm load to ground, so a V_BIAS voltage of +13V is used with additional resistor network circuitry to minimize this additional load. Note that the scope waveform is an attenuated signal (50 Ohm/(450 Ohm = 50 Ohm) or 1/10th of the output signal.

A direct differential probe connection is possible with a TEK P6247 differential high impedance probe (>1GHz bandwidth) on the output LVDS signals at test point J3. The series 453 Ohm resistors (RS1 and RS2) must be removed to allow a clean test point.

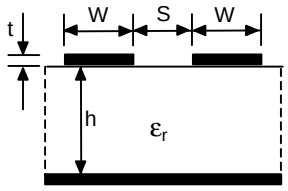
PCB Design

Due to the high speed switching rates obtainable by LVDS a minimum of a four layer PCB construction and FR-4 material is recommended. This allows for 2 signal layers and full power and ground planes. The stack is: signal (LVDS), ground, power, signal. The DS90LV001 demo board is a six layer board of FR-4 material with the following stack: signal (LVDS), ground, power, ground, ground, signal. This stack sandwiches the power plane with two ground planes creating good decoupling capacitance.

Although differential traces are highly recommended for LVDS signals, due to the short distance on this demo board, 50 Ohm single-ended microstrip lines are used. Equations for calculating impedance are contained in National application note AN-905 for both microstrip and stripline PCB traces.

For the microstrip line, the microstrip impedance, Z_O, is:

$$Z_O \cong \frac{6}{\sqrt{0.475\varepsilon_r + 0.67}} \ln\left[\frac{4h}{0.67\,(0.8w + t)}\right] \text{Ohm}$$



For the new evaluation board h = 9 mils, w =15mils and t = 2.1mils. Calculating the impedance, Z_O, is:

$$Z_O \cong \frac{6}{\sqrt{0.475\varepsilon_r + 0.67}} \ln\left[\frac{4h}{0.67\,(0.8w + t)}\right] \text{Ohm}$$

$$\cong \frac{6}{\sqrt{0.475\varepsilon_r\,(4.3) + 0.67}} \ln\left[\frac{4(9)}{0.67\,(0.8(15) + 2.1)}\right] \text{Ohm}$$

$$\cong 48.7 \text{ Ohms}$$

Bypassing capacitors are recommended for each package. A 0.1 µF is sufficient on the buffer device (CB1) however, additional smaller value capacitors may be added (i.e. 0.001 µF at CB21) if desired. Traces connecting V_{CC} and ground should be wide (low impedance, not 50 Ohm dimensions) and employ multiple vias to reduce inductance. Bulk bypassing is provided (C1, close by) at the main power connection as well. Additional power supply high frequency bypassing can be added at CB2, CB12, and CB22 if desired.

Sample Waveforms from the LVDS Evaluation PCB

Single-ended signals are measured from each signal (true and inverting signals) with respect to ground. The buffer ideally switches at the crossing point of the two signals. LVDS signals have a V_{OD} specification of 250mV to 450mV with a typical V_{OS} of 1.2V. Our device has a typical V_{OD} of 325mV, but for the example below, we will use a signal between 1.0 V (V_{OL}) and 1.4 V (V_{OH}) for a 400 mV V_{OD}. The differential waveform is constructed by subtracting the OUT- (inverting) signal from the OUT+ (true) signal. V_{OD} = (OUT+) – (OUT-). The V_{OD} magnitude is either positive or negative, so the differential swing (V_{SS}) is twice the V_{OD} magnitude. Drawn single-ended waveforms and the corresponding differential waveforms are shown in *Figure 5.*

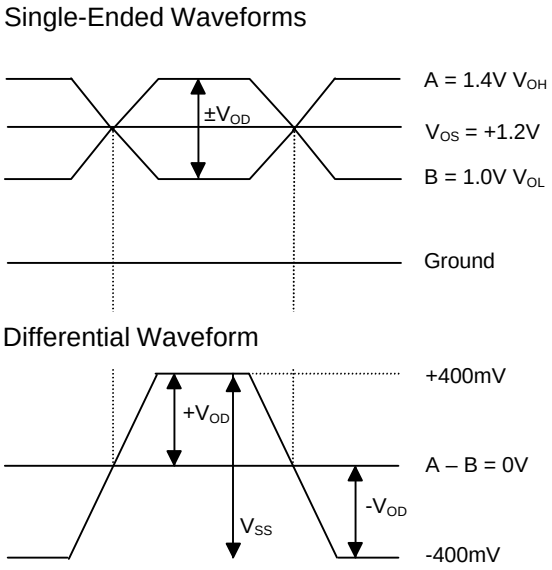
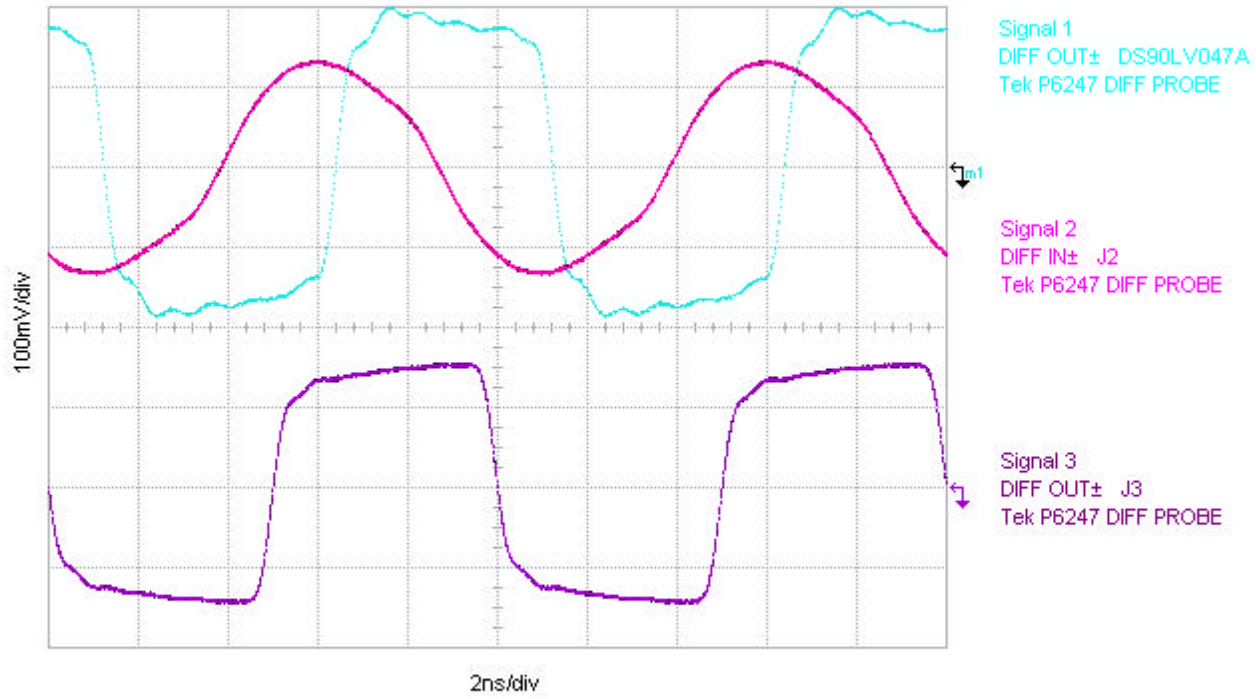


Figure 5: Single-ended and Differential Waveforms

Probing of High Speed LVDS Signals

Probe specifications for measuring LVDS signals are unique due to the low drive level of LVDS (3 mA typical). For this board design, either a 50 Ohm scope module (SD-22) or the TEK P6247 differential probe (>1 GHz bandwidth) must be used. The capacitive loading of the probe should be kept in the low pF range, and the bandwidth of the probe should be at least 1 GHz (4 GHz preferred) to accurately acquire the waveform under measurement.

National's Interface Applications group employs a wide range of probes and oscilloscopes. One system that meets the requirements of LVDS particularly well is an Agilent 86100A Wide-Bandwidth Oscilloscope (>20GHz bandwidth), Agilent 86112 20GHz module and TEK P6247 differential probe heads. The probe offers 200kΩ, 1pF loading and a bandwidth of 1GHz. This test equipment was used to acquire the waveforms shown in *Figure 6.*



Note: 6dB attenuators used to reduce signal amplitude by half

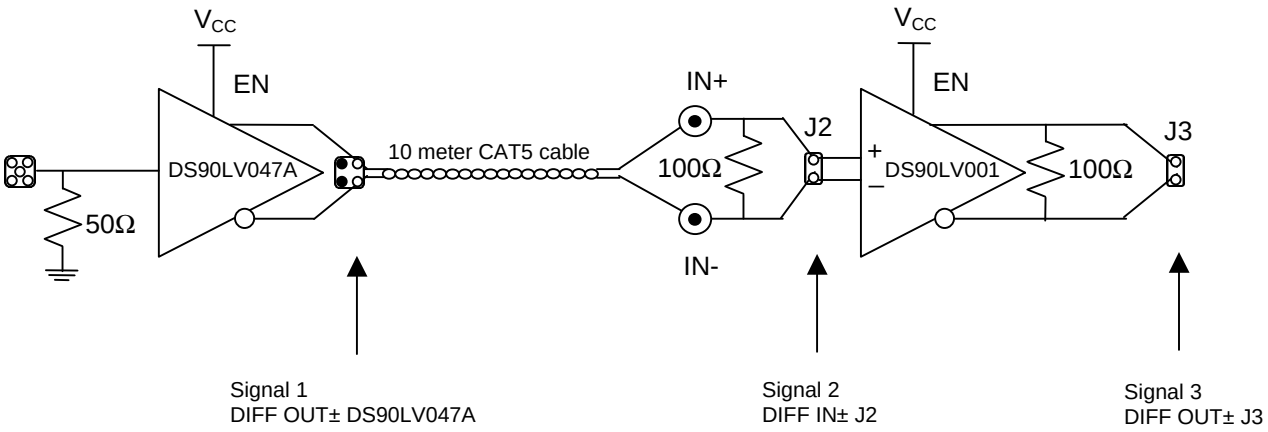


Figure 6: Input and Output LVDS Signals in Cable Repeater Application

In this figure, a DS90LV047A quad LVDS driver was used to drive the DS90LV001 buffer through a 10 meter CAT5 cable. Signal 1 is the differential signal at the output of the DS90LV047A driver. Signal 2 is the differential signal entering the DS90LV001 buffer at the end of the 10 meter cable and signal 3 is the differential output of the DS90LV001 buffer. Note the clean re-driven signal (signal 3), this is the role of a repeater.

Demo PCB Option

Option 1: Disabling the LVDS Buffer

The DS90LV001 buffer features an enable pin. On the evaluation PCB, the active high input (EN) is routed to a jumper (EN). The jumper provides a connection to the V_{CC} plane ("H") or to the Ground plane ("L"). To enable the buffer, connect the jumper to the power plane ("H"), to disable (TRI-STATE) the buffer, connect the jumper to ground ("L").

Note that RT4 is saved for a future use.

Plug & Play

The following simple steps should be taken to begin testing on your completed evaluation board:

1) Connect signal common (ground) to the header marked GND

2) Connect the power supply lead to the header marked VCC (3.3V)

3) Connect +13V to the circuit bias V_BIAS (depending on the resistor tolerances, this voltage should be adjusted to ensure that the output V_{OS} is +1.25V…monitor the voltage at the voltage node before the 1620 Ohm resistor on top of the board…this should be +1.25V)

4) Set EN jumper to the power plane ("H") to enable the buffer

5) Connect a complementary signal by a signal generator to the buffer input (IN- and IN+) with:

   a) frequency = 100 MHz (200 Mbps)

   b) V_{IL} = 1.0V & V_{IH} = 1.4V

   c) t_r & t_f = 2ns

   d) duty cycle = 50% (square wave)

6) Connect a differential probe to test point J2 and either a differential probe to test point J3 or RG142B cables to an SD-22 module to OUT- and OUT+. Do not attempt to connect only one output as the +13V bias voltage assumes that both outputs are loaded with 50 Ohms.

7) View LVDS signals using the same voltage offset and volts/div settings on the scope with the TEK P6247 differential probes and/or SD-22 module and RG142B cables

Summary

This evaluation PCB provides a simple tool to evaluate how the DS90LV001 LVDS – LVDS buffer can be used to regenerate an LVDS signal and to determine signal quality for high speed data transmission applications.

Reference Material

- DS90LV001 datasheet
- LVDS Owner's Manual
- AN-905 Transmission Line RAPIDESIGNER Operation and Application Guide
- AN-1187 Leadless Leadframe Package (LLP)

Additional Information available on the Internet: http://www.national.com/appinfo/lvds

Appendix

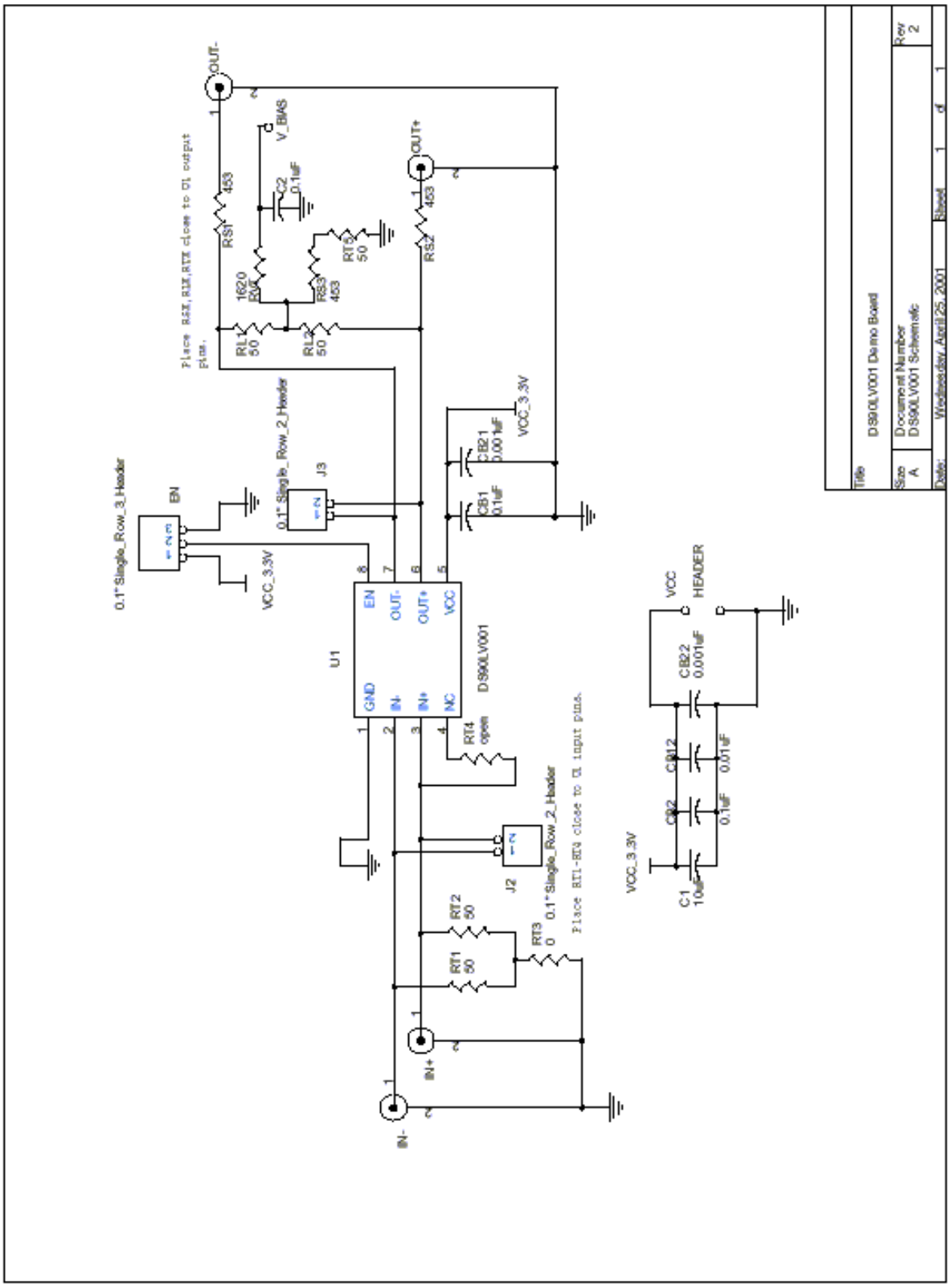
Typical test equipment used for LVDS measurements:

Signal Generator	HP 8133A Pulse Generator
Oscilloscope	Agilent 86100A Wide-Bandwidth Oscilloscope, 86112A 20GHz module
Probes	TEK P6247 differential probe, Tek 1103 TEKPROBE Power Supply
Attenuators	Pasternack 6dB attenuators

Bill of Materials

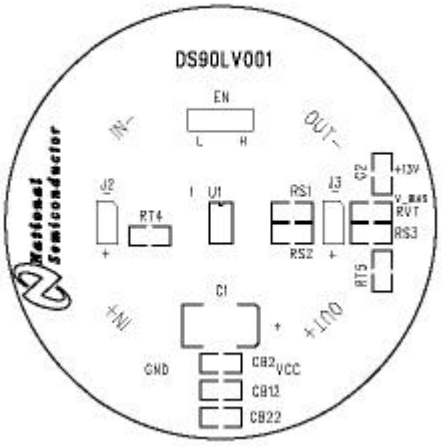
Type	Label	Value/Tolerance	Qty	Footprint	Part Number
IC	U1	(Buffer)	1	8-L SOIC	DS90LV001TM
SMA Jack	IN-, IN+, OUT-, OUT+		4	SMA Connector	Johnson P/N 142-0801-811
Resistor	RT3	0Ω	1	RC0805	
Resistor	RT1, RT2, RT5, RL1, RL3	50Ω	5	RC0805	
Resistor	RS1, RS2, RS3	453Ω	3	RC0805	
Resistor	RVT	1620Ω	1	RC0805	
Resistor	RT4	open	1	RC0805	not loaded
Capacitor	CB1, CB2, C2	0.1µF	3	CC0805	
Capacitor	CB12	0.01µF	1	CC0805	
Capacitor	CB21, CB22	0.001µF	2	CC0805	
Capacitor	C1	10µF, 35V	1	D	Solid Tantalum Chip Capacitor
Headers	EN	3 lead header	1		100 mil spacing (single row header)
Headers	J2, J3	2 lead header	2		100 mil spacing (single row header)
Jumpers		0.1" jumper post shunts	1		
Headers	V_{CC}, GND, V_{BIAS}	1 lead header	3		
PCB			1		LVDS001PCB

Schematic

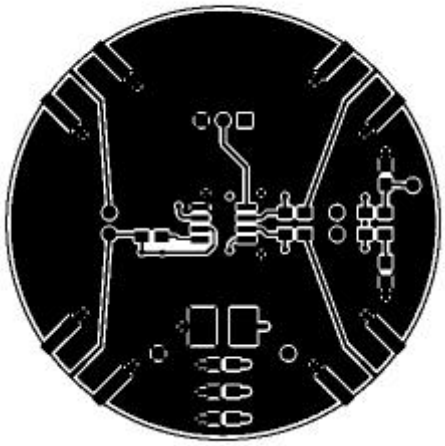

Title
DS90LV001 Demo Board
Size
A
Document Number
DS90LV001 Schematic
Rev
2
Date:
Wednesday, April 25, 2001
Sheet
1
of
1
OUT-
OUT+
IN-
IN+
V_BIAS
C2
0.1uF
RS1
453
RS2
453
RS3
453
RT5
50
1620
5%
RL1
50
RL2
50
Place RS3,RS2,RT5 close to OL output pins.
0.1"Single_Row_3_Header
EN
VCC_3.3V
0.1"Single_Row_2_Header
J3
CB21
0.001uF
CB1
0.1uF
U1
EN
OUT-
OUT+
VCC
GND
IN-
IN+
NC
DS90LV001
RT4
open
J2
RT2
50
RT1
50
RT3
0
Place RT1-RT4 close to OL input pins.
VCC
HEADER
CB22
0.001uF
CB12
0.01uF
CB2
0.1uF
C1
10uF

Demo Board Layers

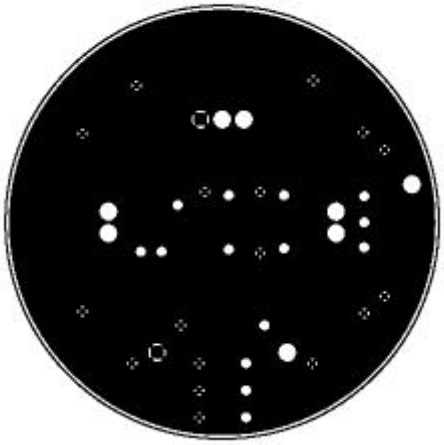
Layer: Silk Top



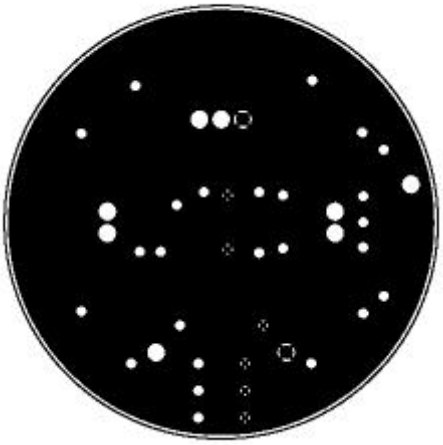
Layer 1: TOP Signal



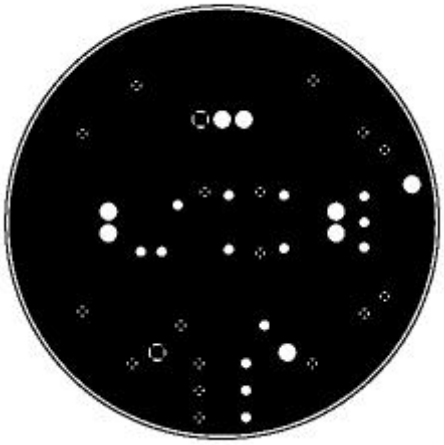
Layer 2: GND



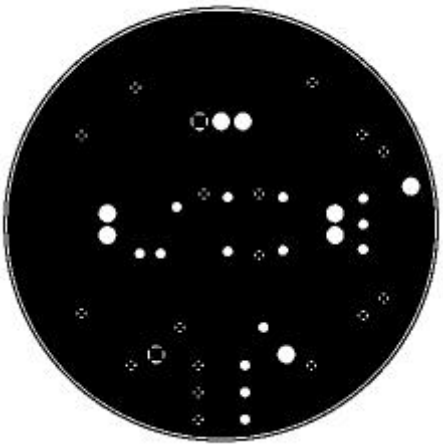
Layer 3: VCC



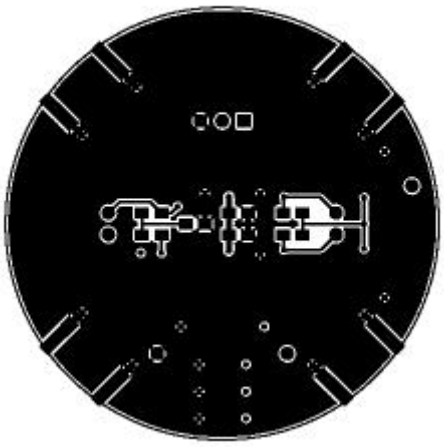
Layer 4: GND



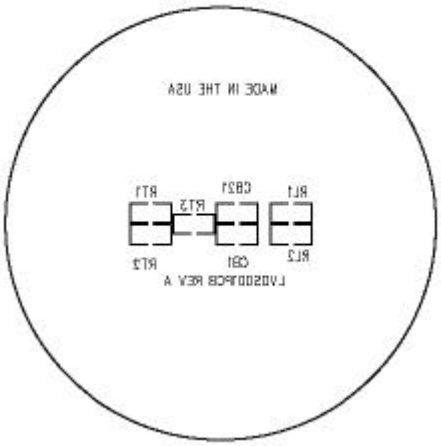
Layer 5: GND



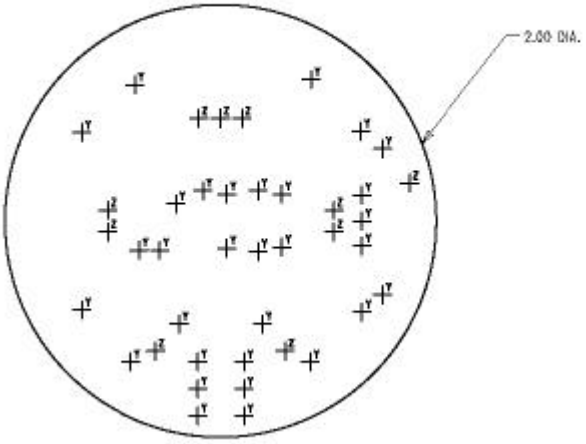
Layer 6: BOTTOM Signal



Layer: Silk Bottom



Fab



Stack up